Appendix E
PAL Listings

```
Name       NBS3.pld;
Partno     NBS3;
Date       9/22/89;
Revision   1;
Designer   b. piatek;
Company    fishcamp;
Assembly   NBS-DIO48;
Location   u8;
Device     P22V10;
Format     j;

/*****************************************************************/
/*      NBS-DIO48 state pal.                                     */
/*                                                               */
/*                                                               */
/*****************************************************************/
/*  Allowable Target Device Types:  22v10                        */
/*****************************************************************/

/**  Inputs  **/

Pin 1        = !clock    ;      /* nubus clock                   */
Pin 2        = !reset    ;      /* nubus reset                   */
Pin 3        = !tm0      ;      /* nubus tm0                     */
Pin 4        = !tm1      ;      /* nubus tm1                     */
Pin 5        = !myslot   ;      /* my nubus slot selected        */
Pin 6        = !start    ;      /* nubus start                   */
Pin 7        = !ack      ;      /* nubus ack                     */
Pin 8        = a19       ;      /* latched nubus a19             */
Pin 9        = a18       ;      /* latched nubus a18             */
Pin 10       = a17       ;      /* latched nubus a17             */

/**  Outputs  **/

Pin 14       = !iowe     ;      /* nubus write 'early' operation  */
Pin 15       = s2        ;      /* msb of state counter           */
Pin 16       = !dio2     ;      /* port 2 address range           */
Pin 17       = !rom      ;      /* onboard rom address range      */
Pin 18       = !dio1     ;      /* port 1 address range           */
Pin 19       = s1        ;      /* s1 of state counter            */
Pin 20       = s0        ;      /* lsb of state counter           */
Pin 21       = !slot     ;      /* latched slot decode            */
Pin 22       = !iow      ;      /* nubus write operation          */
Pin 23       = !ior      ;      /* nubus read operation           */

/** Declarations and Intermediate Variable Definitions **/

FIELD  state_count    =      [s2..s0];     /* state counter bits */
state0                =      !s2 & !s1 & !s0;
state1                =      !s2 & !s1 &  s0;
state2                =      !s2 &  s1 & !s0;
state3                =      !s2 &  s1 &  s0;
state4                =       s2 & !s1 & !s0;
state5                =       s2 & !s1 &  s0;
state6                =       s2 &  s1 & !s0;
state7                =       s2 &  s1 &  s0;
dio1_addr             =      !a19 & !a18 & !a17;
dio2_addr             =      !a19 & !a18 &  a17;
rom_addr              =       a19 &  a18 &  a17;
inten_addr            =      !a19 &  a18 & !a17;
intdis_addr           =      !a19 &  a18 &  a17;
sw_addr               =       a19 & !a18 & !a17;
```

```
/**  Logic Equations  **/

s2.ar          =      'b'0;
s2.sp          =      'b'0;

s1.ar          =      'b'0;
s1.sp          =      'b'0;

s0.ar          =      'b'0;
s0.sp          =      'b'0;


SEQUENCE state_count {

 PRESENT 'h'0
       IF  (myslot & !ack & start & !reset) NEXT 'h'1;
       IF !(myslot & !ack & start & !reset) NEXT 'h'0;

 PRESENT 'h'1
       IF !reset NEXT 'h'2;
       IF  reset NEXT 'h'0;

 PRESENT 'h'2
       IF !reset NEXT 'h'3;
       IF  reset NEXT 'h'0;

 PRESENT 'h'3
       IF !reset NEXT 'h'4;
       IF  reset NEXT 'h'0;

 PRESENT 'h'4
       NEXT 'h'0;

 PRESENT 'h'5
       NEXT 'h'0;

 PRESENT 'h'6
       NEXT 'h'0;

 PRESENT 'h'7
       NEXT 'h'0;

}      /* end of sequence */



iowe.ar=       'b'0;
iowe.sp=       'b'0;
iowe.d         =      start & !ack & myslot & tm1 & !reset
               #      iowe & state1 & !reset
               #      iowe & state2 & !reset;

dio1           =      slot & dio1_addr & !reset;

dio2           =      slot & dio2_addr & !reset;

rom            =      slot & rom_addr & !reset;

slot.ar=       'b'0;
slot.sp=       'b'0;
slot.d         =      start & !ack & myslot & !reset
               #      slot & state1 & !reset
               #      slot & state2 & !reset
```

```
                #       slot & state3 & !reset;

iow.ar          =       'b'0;
iow.sp          =       'b'0;
iow.d           =       iowe & state1 & !reset
                #       iow  & state2 & !reset;

ior.ar          =       'b'0;
ior.sp          =       'b'0;
ior.d           =       start & !ack & myslot & !tm1 & !reset
                #       ior & state1 & !reset
                #       ior & state2 & !reset
                #       ior & state3 & !reset;
```

```
Name       nbs4.pld;
Partno     nbs4;
Date       9/22/89;
Revision   1;
Designer   b. piatek;
Company    fishcamp;
Assembly   NBS-DIO48;
Location   u10;
Device     P22V10;
Format     j;

/*****************************************************************/
/*      NBS-DIO48 decode pal.                                    */
/*                                                               */
/*                                                               */
/*****************************************************************/
/*  Allowable Target Device Types:  22v10                        */
/*****************************************************************/

/**  Inputs  **/

Pin 1        = !clock    ;      /* nubus clock                   */
Pin 2        = int3      ;      /* interrupt 3 line              */
Pin 3        = a17       ;      /* latched nubus a17             */
Pin 4        = a18       ;      /* latched nubus a18             */
Pin 5        = a19       ;      /* latched nubus a19             */
Pin 6        = int1      ;      /* interrupt 1 line              */
Pin 7        = int2      ;      /* interrupt 2 line              */
Pin 8        = s1        ;      /* s1 of state counter           */
Pin 9        = s0        ;      /* lsb of state counter          */
Pin 10       = !slot     ;      /* latched slot decode           */
Pin 11       = !reset    ;      /* nubus reset                   */
Pin 13       = int4      ;      /* interrupt 4 line              */
Pin 14       = s2        ;      /* msb of state counter          */

/**  Outputs  **/

Pin 15       = !intenb   ;      /* interupt enable signal      */
Pin 16       = treset    ;      /* true nubus reset signal       */
Pin 17       = !sw       ;      /* onboard latch address range   */
Pin 18       = !nmrq     ;      /* nubus interupt line           */
Pin 19       = !tm1      ;      /* nubus tm1 signal              */
Pin 20       = !tm0      ;      /* nubus tm0 signal              */
Pin 21       = !ack      ;      /* nubus ack signal              */
Pin 22       = !dclk     ;      /* data strobe                   */
Pin 23       = aclk      ;      /* address strobe                */

/** Declarations and Intermediate Variable Definitions **/

state0               =      !s2 & !s1 & !s0;
state1               =      !s2 & !s1 &  s0;
state2               =      !s2 &  s1 & !s0;
state3               =      !s2 &  s1 &  s0;
state4               =       s2 & !s1 & !s0;
state5               =       s2 & !s1 &  s0;
state6               =       s2 &  s1 & !s0;
state7               =       s2 &  s1 &  s0;
dio1_addr            =      !a19 & !a18 & !a17;
dio2_addr            =      !a19 & !a18 &  a17;
rom_addr             =       a19 &  a18 &  a17;
inten_addr           =      !a19 &  a18 & !a17;
intdis_addr          =      !a19 &  a18 &  a17;
sw_addr              =       a19 & !a18 & !a17;
```

```
s2.oe         =      'b'0;               /* used as an input pin    */


/**  Logic Equations  **/

treset               =      reset;

sw                   =      slot & sw_addr & !reset;

aclk                 =      clock & !slot;

dclk.d               =      state2;
dclk.ar              =      'b'0;
dclk.sp              =      'b'0;

ackoe                =      slot & state4;

ack.d                =      state3;
ack.ar               =      'b'0;
ack.sp               =      'b'0;
ack.oe               =      ackoe;

tm0.d                =      state3;
tm0.ar               =      'b'0;
tm0.sp               =      'b'0;
tm0.oe               =      ackoe;

tm1.d                =      state3;
tm1.ar               =      'b'0;
tm1.sp               =      'b'0;
tm1.oe               =      ackoe;

nmrq                 =      int1
                     #      int2
                     #      int3
                     #      int4;
nmrq.oe              =      intenb;

intenb.d             =      slot & inten_addr & !reset
                     #      intenb & !slot & !reset
                     #      !(slot & intdis_addr) & intenb & !reset;
intenb.ar            =      'b'0;
intenb.sp            =      'b'0;
```